REMARKS

The applicants have carefully considered the Office action dated June 16, 2005 and the references it cites. By way of this Response, claims 1, 17, 20, 24, and 28 have been amended. In view of the following, it is respectfully submitted that all pending claims are in condition for allowance and favorable reconsideration is respectfully requested.

As an initial matter, the applicants note that claims 8, 9, 14-16, 26 and 27 stand allowed and are not discussed in the following.

As a further initial matter, the applicants note that signed copies of the PTO-1449 form from the information disclosure statement mailed June 10, 2003 has not been returned by the Office. The Office is requested to provide the same with the next communication in this application.

Along the same lines of completing the record, the Examiner is asked to make the references cited in the most recent PTO-892 form issued in the continuation application (serial no. 10/303,931) of record in this application to reflect that these references were also considered by the Examiner in connection with this application. A PTO-1449 form identifying these references is attached for the Examiner's convenience.

As a further initial matter, the applicants wish to thank the Examiner for his courteous participation in a telephonic interview with the undersigned on August 26, 2005. During that interview, proposed amendments to the specification and claims and the Chang reference were discussed. The undersigned faxed copies of the proposed amendments to the Examiner to facilitate his consideration of the proposals. The Examiner telephoned the undersigned and indicated that the proposed amendments to claims 24 and 28

would require further searching to fully investigate the patentability issue. The Examiner also indicated that the amendments to the specification did not introduce new matter and would overcome the 35 U.S.C. § 112, first paragraph, rejection of claim 10. Therefore, the applicants are filing this response accompanied by a request for continued examination. This response reflects the proposed amendments with one additional change. In particular, by way of this response, claim 20 has been rewritten in independent form.

Turning to the drawings objections, the applicants respectfully submit that an example "arbitration circuit enforcing a fixed cache priority" is already present in the figures and, therefore, respectfully traverse the drawing objection. In this regard, the Office's attention is respectfully directed toward FIG. 2 which illustrates an example arbitration circuit. In particular, the OR gates 210 and the back-off inputs to the processing agents 200 form an example arbitration circuit enforcing a fixed cache intervention priority between the caches 208. Accordingly, it is respectfully submitted that the drawing objection should be withdrawn.

Turning to the objections to the specification, the applicants respectfully remind the Office that the law does not require the exact claim language to be used in the specification. ("A claimed invention need not be described *ipsis verbis* in order to satisfy the disclosure requirement of 35 U.S.C. Sec. 112." Ex parte Holt, 19 U.S.P.Q.2d 1211, 1213 (B.P.A.I. 1991)). Therefore, the law does not require that the exact terms "a predetermined arbitration hierarchy," "an arbitration circuit," and/or "a predetermined hierarchy" appear in the specification.

Moreover, the objected-to terms find support in the specification and drawings as filed. For example, the paragraph bridging pages 7 and 8 states:

> In addition, one or more of the "hit out" lines are connected to a "back-off" input on each processing agent 200. For one embodiment, a first processing agent 200 optionally includes a "back-off" input which is never asserted (e.g., the input is connected to logic zero). This processing agent 200 has the highest priority in an arbitration scheme described in detail below (i.e., no other agent ever tells this agent to "back-off").
>
> A second processing agent 200 may include a "back-off" input which is connected only to the "hit out" of the first processing agent. This processing agent has the second highest priority (i.e., only the highest priority agent can tell this agent to "back-off").
>
> If included in the system, a third processing agent 200 may include a "back-off" input which is connected to the output of a first OR gate 210. The inputs of the first OR gate 210 are in turn connected to the "hit out" signals of the first processing agent 200 and the second processing agent 200. This processing agent has the third highest priority (i.e., either of the highest priority agent and the second highest priority agent can tell this agent to "back-off").
>
> If included in the system, a fourth processing agent 200 may include a "back-off" input which is connected to the output of a second OR gate 210. The inputs of the second OR gate 210 are in turn connected to the "hit out" signal of the third processing agent 200 and the output of the first OR gate 210. This processing agent 200 has the fourth highest priority (i.e., any of the first three agents can tell this agent to "back-off"). This pattern may continue for any number of processing agents 200 as shown in FIG. 2.

Thus, the specification and FIG. 2 clearly disclose an example arbitration circuit enforcing a fixed cache intervention priority between the caches 208, namely, the OR gates 210 and the back-off inputs to the processing agents 200. This arbitration circuit defines a predetermined arbitration hierarchy between the caches of the processing agents. Therefore, it is respectfully submitted that the objected-to terms are supported by the specification and drawings as filed.

Similarly, the amendments made to the specification and claims via this paper are fully supported in the application specification and drawings as filed. For example, the example circuit of FIG. 2 is unmistakably hardware that enforces a fixed arbitration hierarchy. This example arbitration hierarchy is both physically determined and permanent. Therefore, it is respectfully submitted that the amendments to the specification and claims proposed herein are fully supported by the original application materials and do not introduce new matter into the application.

Turning to the art rejections, the Office action rejected claims 1-7, 17-25 and 28-32 as being unpatentable over one or more of Chang, U.S. Patent 6,519,685 (also assigned to Intel, the assignee of the instant patent application) and O'Leary, U.S. Patent 5,867,162. The applicants respectfully traverse these rejections.

At the outset, the applicants note that, because at the time the invention of this application was made, Chang and the instant application were assigned to and/or under an obligation to be assigned to Intel Corporation, Chang is not prior art under 35 U.S.C. § 103. Therefore, the 35 U.S.C. § 103 rejections of claims 20-23 are in error as a matter of law and must be withdrawn.

In view of this error, claim 20 has been rewritten in independent form to include the recitations of its base claims. Claim 20 and all claims depending therefrom are in condition for allowance. Because rewriting claim 20 in independent form does not change its scope in any way, no narrowing amendment has been made to claim 20 and none of the amendments to claim 20 were necessary for patentability. Accordingly, the amendments to claim 20 do not give rise to prosecution history estoppel.

The only remaining art rejections are the 35 U.S.C. § 102(e) rejections of claims 1-7, 17-19, 24, 25 and 28-32 based on Chang. Applicants respectfully traverse these rejections.

Claim 1 is patentable over the art cited in the Office action. Claim 1 recites a method of cache intervention comprising providing a copy of a memory block to a third cache from an arbitration winner cache selected based on a fixed hardware arbitration hierarchy. Although Chang discloses a cache coherency protocol, Chang does not disclose a fixed hardware arbitration hierarchy to determine which of at least two caches will intervene to provide a shared memory block to a third cache.

On the contrary, in the cache coherency protocol defined by Chang the intervention priority of the caches changes from situation to situation (see, for example, FIGS. 4A-4B of Chang where the caching agents 2-3 contend for the shared-respond state, and Col. 9, lines 36-39 indicating that "the first caching agent ... to issue a read bus cycle" enters the shared-respond state, thereby indicating that the cache intervention priorities between the caches are not fixed or permanent, but instead change over time). Therefore, the Shared-Respond" cache is not selected in accordance with a fixed hardware arbitration

hierarchy as recited in claim 1, but instead, the Shared-Respond cache is selected in real time based on a performance criterion. Accordingly, Chang does not teach the combination recited in claim 1. As discussed above, Chang is not available as a reference under 35 U.S.C. § 103. Accordingly, claim 1 and all claims depending therefrom are allowable over Chang.

Claim 10 is also allowable. Claim 10 was not rejected on the art, but was only rejected under 35 U.S.C. § 112, first paragraph. As discussed above, that § 112, first paragraph, rejection has been overcome, because an example arbitration circuit as recited in claim 10 was clearly disclosed in at least FIG. 2 and the corresponding text of the application as originally filed. Thus, claim 10 and all claims depending therefrom are allowable.

Independent claim 17 is also allowable. Claim 17 recites a computer wherein a first microprocessor or a second microprocessor provides a copy of a memory block to a cache of a third microprocessor based on a physically predetermined arbitration hierarchy. As discussed above, Chang does not teach a physically predetermined arbitration hierarchy. Accordingly, claim 17 and all claims depending therefrom are allowable.

Independent claim 24 is also allowable. Claim 24 recites a method comprising selecting a first cache or a second cache to provide a copy of a memory block to a third cache based on a permanent hierarchy between the first and second caches. As discussed above, Chang does not teach such a method. Accordingly, claim 24 and all claims depending therefrom are allowable.

Independent claim 28 is also allowable. Claim 28 recites a method of cache intervention comprising preventing a third cache from supplying a copy

of a memory block to a second cache if a first cache has a higher cache intervention priority under a fixed hierarchy defined between the first and second caches. As discussed above, Chang does not teach such a method. Accordingly, claim 28 and all claims depending therefrom must be allowed.

If the Examiner is of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is invited to contact the undersigned at the number identified below.

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